REMARKS

The following remarks are made in response to the Non-Final Office Action mailed April 22, 2008. Claims 43 and 45 have been withdrawn from consideration. Claims 22-42 and 44 were rejected. With this Response, claims 22, 41 and 44 have been amended. Claims 22-25, 27-37, 39-42 and 44 remain pending in the application and are presented for reconsideration and allowance.

Election/Restrictions

A Restriction Requirement was set forth relative to the Examiner-identified inventions of Group I (claims 1-42 and 44) and Group II (claims 43 and 45). Applicant hereby confirms the election of Group I, consisting of at least claims 1-42 and 44.

In the Specification

The Examiner objected to the title because it is not descriptive. Applicant has amended the title to correct this informality.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 22, 33-35, 40-41, and 44 under 35 U.S.C. § 102(e) as being anticipated by the Farnworth et al. U.S. Patent No. 6,515,325. With this response, Applicant has amended claims 22, 41 and 44 such that the claims are not taught or suggested and thus are in condition for allowance.

As amended, claim 22 is a vertically integrated field-effect transistor including a first electrically conductive layer, a middle layer, formed partially from dielectric material, on the first electrically conductive layer, a second electrically conductive layer on the middle layer, and a nanostructure integrated in a via hole introduced into the middle layer. The nanostructure includes a first end portion that is coupled to the first electrically conductive layer and a second end portion that is coupled to the second electrically conductive layer. The first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region of the field-effect transistor.

The middle layer, between two adjacent dielectric sublayers, has a third electrically conductive layer, the thickness of which is less than the thickness of at least one of the dielectric sublayers. A ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein. Within each of the dielectric sublayers, ***a region in the via hole between the nanostructure and the respective dielectric sublayer is free of electrically insulating material***.

Support for the amended claims can be found at least in Figure 1A and paragraphs [0083] and [0084] of the specification of the Graham U.S. Patent Application Publication No. 2006/0128088. Figure 1A illustrates that within the dielectric sublayers 102a and 102b, a region in the via hole 108 between the nanostructure 104 and the respective dielectric sublayer 102a/b is ***free of electrically insulating material***. Clearly, the field affect transistor 100 illustrated in Figure 1A has a gap between the nanostructure 104 and the walls of the via hole 108 within the dielectric sublayers 102a/b, in contrast, for example, to the field effect transistor 200 illustrated in Figure 2, in which the insulating ring structure is replaced by an electrically insulating boundary coating 201 that clearly fills the gap between the nanostructure 104 and the walls of the via hole (cf. paragraphs [0083] and [0084]).

In contrast to the subject matter claimed in amended claim 22, the Farnworth reference does not disclose that within each of the dielectric sublayers, a region in the via hole between the nanostructure and the respective dielectric sublayer is free of electrically insulating material. In the field-effect transistor device 70 illustrated in Figure 5 of the Farnworth reference, the sub regions of insulating layer 20 above, below and between gates 79 and 81 are formed directly on nanotube 22. As such, there is no region free of electrically insulating material left in the via hole between nanostructure 22 and the insulating material of layer 20 within regions A, C and E (as denoted by the Examiner). Moreover, the Farnworth reference does not suggest that a region free of electrically insulating material (clearly, a gap) may be left between the nanostructure 22 and insulating regions A, C and E in the transistor 70. In fact, the Farnworth reference merely discloses (in connection with related embodiments) that an insulating layer is formed (deposited)

over a pre-grown nanotube (see col. 5, lines 29 to 34 and Figure 2G; col. 7, lines 1 to 3 and Figure 4C) and thus abuts the nanotube. However, in no case a region free of electrically insulating material is left in the via hole between the nanostructure and the insulating layer.

Consequently, the subject matter of claim 22 is not taught or suggested by the Farnworth reference and is thus novel and non-obvious over it. Furthermore, independent claims 41 and 44 have been amended similarly and are allowable for the reasons given above. Dependent claims 33-35 and 40 ultimately depend from claim 22 and recite further limitations. Thus, the subject matter of these claims is novel and non-obvious over the Farnworth reference for at least the same reasons.

Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 102(e) rejection to the claims, and request allowance of these claims.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 22-25, 27-28, and 30-43 under 35 U.S.C. § 103(a) as being unpatentable over the Mancevski U.S. Patent Publication No. 2001/0023986 in view of the Choi et al. U.S. Patent Publication No. 2002/0001905. Also, the Examiner rejected claim 29 under 35 U.S.C. § 103(a) as being unpatentable over the Mancevski U.S. Patent Publication No. 2001/0023986 in view of the Martin et al. U.S. Patent Publication No. 2001/0019279. Applicant respectfully disagrees that the claims as amended are taught or suggested by these references, either alone or in combination.

As acknowledged by the Examiner of page 11 of the Office Action, the Mancevski reference fails to disclose an electrically insulating ring structure as gate-insulating region of the field-effect transistor, arranged in a third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein. In fact, the Mancevski reference neither discloses nor suggests providing any gate-insulating region at all.

The Choi reference discloses a vertical field-effect transistor (Fig. 1) having a vertically grown carbon nanotube 100 as a channel arranged in a hole 10' and a nonconductor film 30 that electrically insulates the nanotube 100 from a gate 20 of the transistor. The nonconductor film

30 is deposited onto the hole 10' thereby filling the entire hole 10' with electrically insulating material of the non-conductor film 30. As such, the nanotube 100 abuts the non-conductor layer 30 such that there is no region free of electrically insulating material left between the nanotube 100 and non-conductor film 30.

Even assuming for the sake of argument that one would be motivated to combine the Mancevski and Choi references (a proposition Applicant does not concede), the claim is still not taught or suggested. That is, even if a gate-insulating region from the Choi references is provide in the transistor structure of the Mancevski reference, a non-conductor film would be deposited over the via holes disclosed in the Mancevski reference such that the holes are entirely filled with electrically insulating material that abuts the nanotubes. As such, the combination would end up teaching a structure that is different from the field-effect transistor structure claimed with amended claim 22, which recites that within each of two adjacent dielectric sublayers a region in the via hole between the nanotube and the respective dielectric sublayer ***is free of electrically insulating material***.

Consequently, claim 22 as amended, (and claim 41, which has been amended similarly) is not taught or suggested by the Mancevski reference in view of the Choi reference for at least the reasons given above. Claims 23-25, 27-28, 30-40, and 42 are ultimately dependent on one of claims 22 and 41 and recite further limitations. Thus, they are believed to be non-obvious over the Mancevski reference in view of the Choi reference for at least the same reasons. Furthermore, claim 29 is also is ultimately dependant on claim 22, and it too is thus in allowable form.

Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection to the claims, and request allowance of these claims.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 22-25, 27-37, 39-42 and 44 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 22-25, 27-37, 39-42 and 44 are respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Paul P. Kempf at Telephone No. (612) 767-2502, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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